The Physical Layer in the CAN FD world

Magnus-Maria Hell, Infineon Technologies

The new CAN format CAN FD (CAN with flexible data rate) allows to increase the data rate in the data phase up to 10 MBit/sec. Existing CAN transceivers and additional components for ESD and emu improvements are specified up to 1MBit/sec and for higher bit rates the requirements especially for the transceiver have to be analyzed. This report will give an answer to this question.

Introduction

In existing classical CAN networks, bit rates of 125kBit/sec, 250kBit/sec, and 500kBit/sec are typical data rates in the automotive world. In the industrial area lower bit rates down to 50kBit/sec and higher bit rates up to 1MBit/sec are used. According to this, transceivers are specified up to 1MBit/sec only. The ISO specifications 11898-2/-5/-6, which are relevant for the physical layer, are specified up to 1 MBit/sec. With CAN FD, the data rate can be increased in the data phase. At the moment 2 MBit/sec in bigger networks and up to 5MBit/sec in point to point communication are in discussion. The impact on the physical, which includes the transceiver, the network and the interface between microcontroller and transceiver, will be discussed in this article.

The physical layer

In ISO 11898-2/-5 and -6, a lot of static parameters are specified e. q. recessive level and the $_{\text{dominant}}$ voltage level. For higher bit rates dynamic parameters are more important. The only one dynamic parameter for the physical layer is the TxD to RxD propagation delay (loop delay) with a maximum value of 280 ns in the ISO 11898-2 and 255ns in the ISO 11898-5. The ISO 11898-6 based on the ISO 11898-5 and the propagation delay specification was untouched. This propagation delay is specified for the transceiver with a defined load, but in real application additional delays have to be taken into account like:

- Delay between microcontroller and transceiver
- Delay of components improving the esd and emc robustness.
- Ringing especially at the end of the dominant to recessive edge

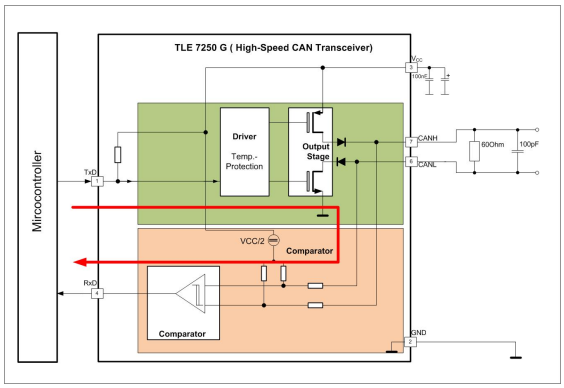

Figure 1: TxD to RxD Transceiver Propation delay specification

The TxD to RxD loop delay is valid for the recessive to dominant transition as for the dominant to recessive transition also. The parameter is specified for a bus load of 60Ω and 100pF. The disadvantage of this specification is that it allows a very asymmetric propagation delay for both transitions. This can shorten or expand the bit length of the recessive or dominant bits and limits the maximum possible bit rate in the data phase.

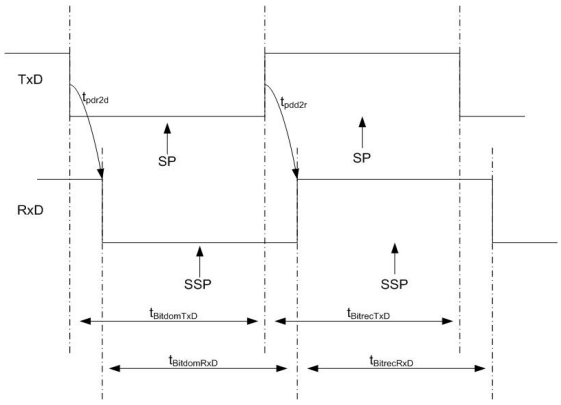

Figure 2: Transceiver with a perfect symmetric TxD to RxD propagation delay

Propagation delay symmetry.

Figure 2 shows a very symmetric TxD to RxD propagation delay performance. The RxD bit time of the dominant bits is the same like the bit time of the TxD bits. In Figure 3 a very asymmetric behavior is shown. The dominant bit of RxD is extremely shortened and the recessive bit of RxD is expanded.

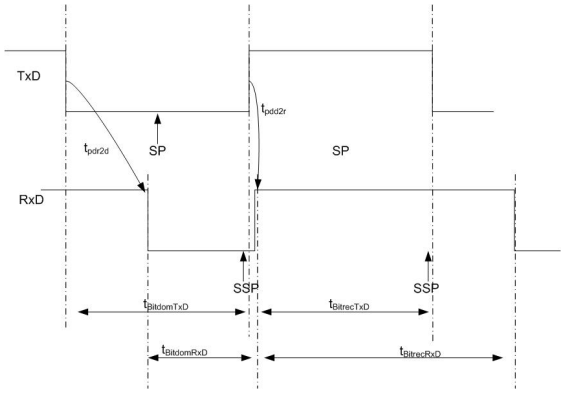

Figure 3: Transceiver with a very asymmetric propagation delay TxD to RxD

Such an extreme asymmetry limits the minimum possible bit time and the maximum possible bit rate. To optimize the transceiver behavior for CAN FD applications the propagation delay symmetry will be now specified. During analyses of several CAN transceivers on the market, we found out, that the number of dominant bits in a row has an impact on the transceiver behavior. To cover this observation in the specification the bit time of the recessive bit after 5 dominant bits in a row is specified. Normally, lower bit rates

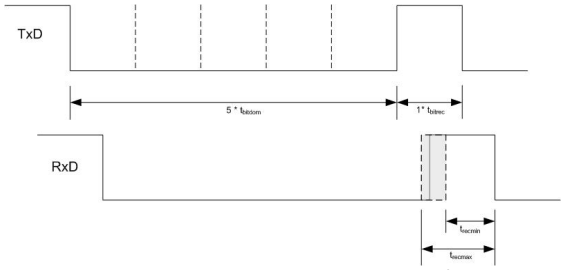

Figure 4: propagation delay specification for CAN FD transceiver

have no impact on this performance. This specification can be used for lower bit rates too. Two different bit rates for the data phase are in discussion at the moment: 2 MBit/sec for communication in complex networks and 5 MBit/sec for point to point communication. For higher bit rate a higher precision is needed. That is the reason why for 2 MBit/sec and for 5MBit/sec different limits are specified. To cover this specification with the one kind of transceiver the temperature range and the 5V supply (VCC) range are tailored. The advantage

Table 1: Specification for the TxD to RxD propagation delay symmetry

Recessive bit time	t_{recmin}	t_{recmax}
2MBit/sec 4.75V< VCC<5.25V -40°C ≤ T_j ≤ 150°C	400ns	550ns
5MBit/sec 4.85V< VCC<5.15V -40°C ≤ T_j ≤ 105°C	120ns	220ns

of this specification is that it can be used for lower bit rates too. For all lower bit rates the recessive bits will be shortened up to 100ns and can be expand up to 50ns. These values can now be used for the network and sample point calculation in the arbitration phase too.

Another reason for asymmetric delay is the physical behavior of the bus network itself. CAN transceiver have open drain output stages (see Figure1) and no push pull power stages for example like Flexray transceivers have. This open drain concept allows controlling the recessive to dominant slew rate to optimize the emission and allows controlling the dominant level on the bus only. For the dominant to recessive transition the maximum slew rate will be controlled by the output stages, but the minimum possible slew rate is dominant by the bus. In case of a high capacitive load, resulting from a high number of nodes and/or of additional external ESD or emu components, the dominant to recessive transition time can be increased and reduces the bit time of a recessive bit. Figure 5 shows the impact of two different capacitive loads. On top of Figure 5 the bus differential voltage behavior with a capacitive load of 220pF is shown and on the bottom side the same curve for a capacitive load of 1.5nF is shown. Both edges have a smaller slew rate but the

dominant bit is expanded. The length of the dominant bit

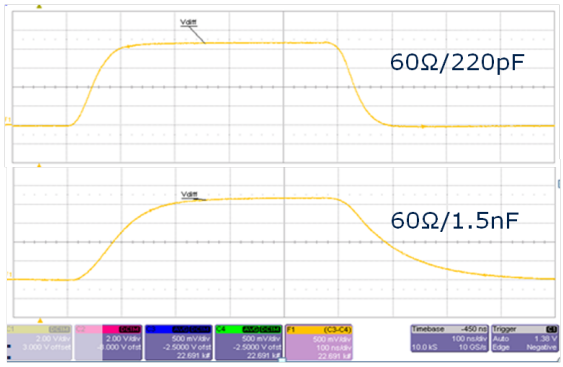

Figure 5: The impact of different capacitive load on the dominant bit time

time depends on the threshold levels of the receiver like implied in Figure 6. A

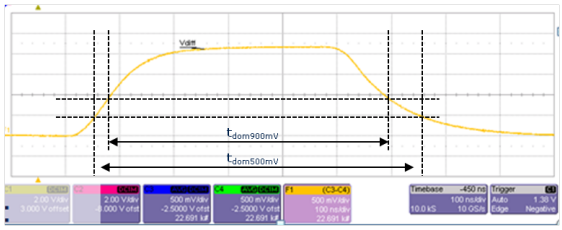

Figure 6: The maximum and minimum receiver threshold levels are marked

receiver with a high threshold (900mV) detects a smaller dominant bit time as a receiver with the minimum possible threshold.

Further reasons for variation

Further reason for the asymmetry of the propagation delay is the temperature. Depending on the technology and the driver concept, the temperature coefficient can be positive or negative. The second reason for the variation of the asymmetry is the dominant differential voltage (V_{CANH}-V_{CANL}) level. If the dominant voltage level is high, for example close to the maximum level of 3V, the switch off time is longer, until the differential voltage level is below the minimum receiver threshold level of 500mV. The dominant differential voltage level depends on

- fabrication variation of the Ron of CANH and CANL
- temperature
- VCC 5V supply variation

For higher bit rates the VCC range and the temperature range are tightened to achieve a stable communication for higher bit rates too.

Microcontroller to Transceiver interface

The interface between microcontroller and transceiver can also be a reason for asymmetric delay. The slew rate symmetry of the TxD output driver of the microcontroller and the slew rate symmetry of the transceiver RxD output driver have an impact on the symmetry too. The capacitive load on the board as well as the capacitive input load of the transceiver TxD input or the microcontroller RxD input can modify the symmetry. Especially the input concept of the transceivers TxD input buffer like CMOS level input or TTL level input threshold can lead to additional asymmetry. The CMOS level input has less impact of the symmetry if the slew rates of the output driver are perfectly matched. The asymmetry is dominated by the symmetry performance of the driver. If the transceiver TxD input has TTL input levels these thresholds adds an additional asymmetry created by the thresholds itself. Figure 7 shows an

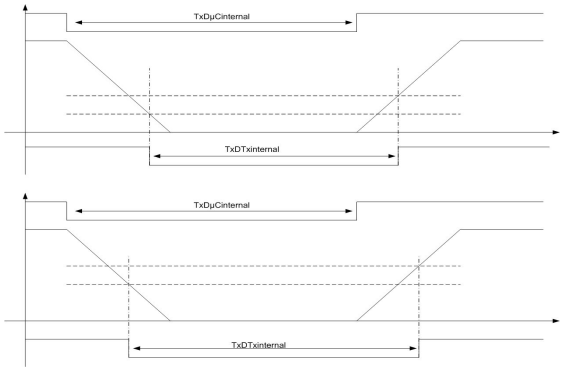

Figure 7: Comparison of TTL or CMOS transceiver TxD input concept

example with a very low input threshold and a very small hysteresis. The slew rates of the driver are very symmetric, but the dominant bit time will be shortened by the TTL input stage. This asymmetry can be helpful, because it expands the recessive bit while normally the bus reduces the recessive bit time. In point to point networks with a termination at both ends, this limits the bit rate too. In Figure 8 the impact of asymmetric signals on the

transceiver TxD input is shown. Asymmetric signals especially at high capacitive loads modifies the bit time of the recessive and dominant bits too. Therefore, the receiver and the microcon-

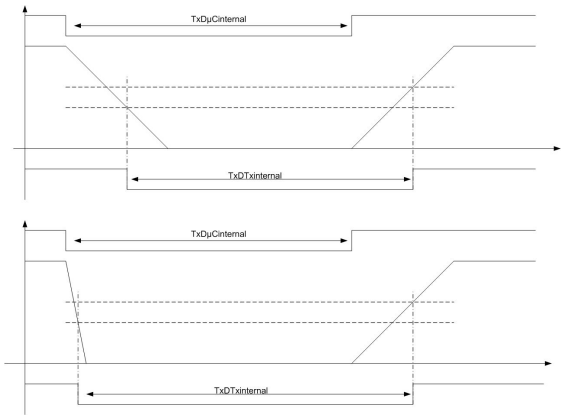

Figure 8: The impact of the transceiver internal bit time depends on the slew rate

troller output drivers have to be symmetric especially for high capacitive loads.
In isolated applications with an Optocoupler as interface between microcontrollers and transceiver, the propagation delay of the Optocoupler has to be into account. Optocoupler have an

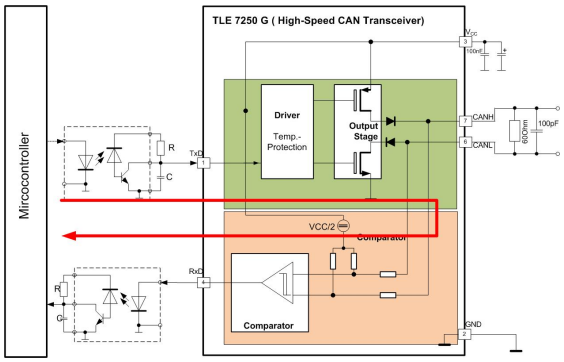

Figure 9: Optocoupler as interface for isolation

open drain output stage. The high to low (recessive to dominant) edge is driven by the output transistor. The dominant to recessive edge depends on the external RC circuit.

Reflections

Furthermore a reason for asymmetry is the ringing at the dominant to the recessive transition. To remember, this is the uncontrolled transition.

Not terminated wires and star topologies are the reason for ringing at this transition. This ringing shortens the recessive bit too. The recessive to dominant transition is less critical because the transceiver controls this transition with its output stages. If a ringing is present it is damped by the powerful output stages.

Sampling point

Why is symmetry of the physical layer so important? The asymmetry of the physical layer reduces the possible range for the sampling point. If we have a look on the latest possible sampling point time than two different scenarios have to be checked. Scenario 1 is the maximum possible distance between two recessive to dominant edges to synchronize again. This time is 10 bit times. To calculate the latest possible sampling point the

- Oscillator tolerance of sender and receiver
- SJW
- Asymmetry of microcontroller and transceiver interface

have to be into account.
The second scenario is the 5 Bit scenario with the maximum number of dominant bits in a row. In this scenario the

- Oscillator tolerance
- The transceiver asymmetry (50ns for 2 MBit/sec and 20ns for 5Mbit/sec)
- SJW
- Asymmetry of microcontroller and transceiver interface

have to be analyzed. For the earliest possible sampling time, the recessive bit after 5 dominant bits is the most critical scenario. In this scenario the

- Oscillator tolerance
- The transceiver asymmetry (100ns for 2 MBit/sec or 80ns for 5Mbit/sec)
- SJW
- Asymmetry of microcontroller and transceiver interface
- Network ringing and bus load

have to be taken into account.

Summary

To get a successful and stable communication with CAN FD

- CAN FD transceiver should be used
- A linear network with small stubs is recommended
- Small capacitive bus loads are mandatory
- Small capacitive loads on the ECU are recommended

An intensive analysis of the sampling point is necessary also. The new parameter for transceiver will be helpful for classical CAN networks and for CAN FD networks too. For classical CAN networks these parameter help to calculate the sampling point easier or with a more reliability. No values must be evaluated or estimated by you they will be given in future datasheets. The standardization will be started at the beginning of 2014. The ISO 11898-2/-5 and-6 parts will be harmonized and the new parameter will be added. A final new ISO 11898-2 specification is expected until end of 2014. Infineon will start the investigation on existing CAN transceiver and add this new parameter in the datasheets.

Magnus-Maria Hell
Infineon Technologies AG
Am Campeon 1-12
DE-85579 Neubiberg
Tel.: +49-89-234-24003
Magnus-Maria.Hell@infineon.com
www.infineon.com

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